REMARKS

The examiner has rejected claims 2, 6, 12 and 16 on the basis of certain formalities. In particular, the examiner contends that the claimed function sets the image exposure time of the specific row and not the image exposure time of the entire semiconductor imaging chip. In response, applicant has amended claims 2, 6, 12 and 16 to correct the informality. Claims 8 and 18 have been similarly amended. In addition, claims 1, 4, 8, 11, 14 and 18 have been amended to indicate the time sequence in which a row is accessed for a second time.

The examiner has rejected all claims. Claims 4 and 14 are rejected as being anticipated under 35 USC 102(e) and the remaining claims are rejected as obvious to one of ordinary skill in the art under 35 USC 103(a) using various combinations of three cited references, namely, US patents 6,218,656 and 6,587,146 to Guidash and U.S. patent 6,529,242 to Panicacci. Claim rejections are as follows:

Claim	Guidash '656	Guidash '146	Panicacci '242
4, 14	X		
1, 5, 11 and 15	X	X	
2, 3, 12 and 13	X	X	X
6-9 and 16-19	X		X
10, 20	X	X	X

The first filed Guidash patent ('146) describes the known technique of correlated double sampling (CDS) for eliminating pattern noise in photodiode arrays. Pattern noise is caused by variations in the source follower offset values in different APS (active pixel sensor) cells. In Guidash '146, the pixel signal value and the pixel reset value are sequentially stored and

then subtracted from each other in a differential column buffer. However, Guidash '146 uses separate access and reset lines.

The second filed Guidash patent ('656) describes a technique for eliminating the row select transistor in a 4-transistor cell to create a 3-transistor cell. As stated in the Summary of the Invention,

> "The present invention provides a high fill factor Photodiode Active Pixel Architecture with the capability to perform Correlated Double Sampling, (CDS). The functionality of a 4 transistor pixel is maintained while eliminating the separate row select transistor. This is done by sharing the RG control signals in one row with the row select means of an adjacent row." (Guidash '656, column 2, lines 32-38)

However, Guidash '656 fails to use the merged reset and row select signals to perform the claimed method of eliminating pattern noise. Instead, Guidash '656 provides a transfer gate buss for each row (Guidash '656, figure 2, reference numerals 26 in cells i and i-1). The transfer gate performs the equivalent function of a row select signal. The transfer gate in figure 2 moves the stored charge representing the pixel signal value to the source follower FET transistor which is connected to the column output signal buss.

In particular, Guidash '656 shows in the timing diagram of figure 3, that each row is accessed twice before moving on to the next row: once to get a reset level (using SHR), and a second time to get a signal level (using SHS). In between the two readings, Guidash '656 operates the transfer gate (TGi). Figure 3 illustrates 3 rows: i-1, i and i+1. All operate the same:

For cell i-1: first SHR, then TGi-1, then SHS, moving on to the next row,
For cell i: first SHR, then TGi, then SHS, moving on to the next row
For cell i+1: first SHR, then Tgi+1, then SHS, moving on to the next row

As can be seen, Guidash '656 accesses both of the reset and signal level photocell values for a given row, before moving on to the next row. Specifically, for each row in figure 3, Guidash '656,

1) operates the reset gate RG
2) samples the reset level SHR
3) operates the transfer gate TG
4) samples the signal level SHS.

Guidash then moves on to the next row. The availability of the transfer gate (TG) makes the actual operation of the device not significantly different from that of an active pixel sensor that did not merge the access/reset row lines. Guidash '656 really only shows the elimination of one transistor in the pixel configuration as his innovation.

THE CLAIMED SUBJECT MATTER

In contrast, applicant's claims are directed to a method and apparatus for canceling pattern noise not show or suggested by either Guidish '146 or '656. Claims 1, 4, 8, 11, 14 and 18 have been amended to clarify the time sequence: i.e., access row N, then access row N+1 and thereafter, access row N for a second time. All of the independent claims contain the kernel of this concept not shown by Guidash.

For example, as set forth in claim 4, Guidash does not show or suggest,

"accessing row N of said array a first time;

accessing row N+1 of said array, said row N of said array being the previous row to said row N+1 of said array; and thereafter

accessing row N of said array a second time."

Similarly, as set forth in claim 14, Guidash does not show or suggest,

a first row driver for accessing row N of said array a first time;

a second row driver for accessing row N+1 of said array, said row N of said array being the previous row to said row N+1 of said array; and

a scan controller coupled to said first row driver for thereafter accessing row N of said array a second time.

As set forth in claim 1, Guidash does not show or suggest,

accessing a first row of said array to obtain a first sample of said given active pixel sensor output;

storing said first sample of said given active pixel sensor output of said first row of said array;

accessing a second row of said array, said first row of said array being the previous row to said second row of said array; and thereafter,

accessing said first row of said array a second time to obtain a second sample of said given active pixel sensor output;

storing said second sample of said given active pixel sensor output of said first row of said array; and

subtracting said second sample from said first sample to form said corrected output from said given active pixel sensor.

Similar claim language, indicating the time sequence in which a given row N is accessed for a second time, is found in applicant's independent claims 1, 4, 8, 11, 14 and 18. Guidash does not show or suggest the cancellation of pattern noise using the claimed time sequence. The dependent claims are patentable for the same reasons as the independent claim upon which each respectively depends.

As a secondary indicia of the non-obviousness of canceling threshold variations in a simple 3 transistor APS pixel array, when the access line of the current row is merged with reset line of the previously read row, applicant separately submits the prior art article, "A Pixel Size Shrinkage of Amplified MOS Imager with Two-line Mixing", Yamawaki et. al. IEEE Transactions on Electron Devices, Vol 43, No 5, May 1996, pp 713-719. The performance of the Yamawaki et al imager is limited by threshold variations, which are discussed in the above cited article at some length. There is no attempt or mention of on chip cancellation of pattern noise. At the time, it was widely considered impossible to cancel the pattern noise in a simple 3-transistor cell with merged access and reset lines.

Applicant has made an earnest effort to present claims patentably distinct from the references, and point out how the specific language of the claims patentably distinguishes such references.

For the foregoing reasons, applicant urges reconsideration of the amended claims. It is respectfully requested that the examiner withdraw the rejection of claim and pass the present application to issue.

Respectfully submitted,
by

DATED: Sept 15, 2004

ALLAN J. JACOBSON
Attorney for applicant
Registration No. 29,079
13-310 Summit Square Center
Langhorne, Pennsylvania 19047
telephone:(215) 579-1426